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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/559,190	04/27/2000	Richard M. Wyatt	2037.2002-000	2260

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HAMILTON, BROOK, SMITH & REYNOLDS, P.C.
530 VIRGINIA ROAD
P.O. BOX 9133
CONCORD, MA 01742-9133

EXAMINER	
WILSON, ROBERT W	

ART UNIT	PAPER NUMBER
2661	

DATE MAILED: 08/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/559,190	WYATT, RICHARD M.	
	Examiner	Art Unit	
	Robert W. Wilson	2661	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 7/22/05.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-45 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-3,5,12-15,17,24-28,30,37-39 and 41-45 is/are rejected.

7)☒ Claim(s) 4,6-11,16,18-23,29,31-36 and 40 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 23 August 2000 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3, 5, 12-15, 17, 24-28, 30, 37-39, 41-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Runaldue (U.S. Patent No.: 6,128,654).

Referring to claim 1, Runaldue teaches: Output Queue 74 and Transmit FIFO 54 per Fig 3 or per col. 7 lines 34-52 which are a queue. The Output Queue 74 per Fig 3 or per col. 7 lines 34-52 is the first memory. The Transmit FIFO 54 per Fig 3 or per col. 7 lines 34-52 is the second memory. The Port FIFO logic writes the pointer into the Output Queue or first memory per col. 7 lines 34-52. The Buffer Manager writes the pointer into the Transmit FIFO or second per memory per col. 7 lines 34-52. Runaldue does not expressly call for: different access times associated with the Output Queue and the Transmit FIFO or dequeuing of the pointer.

It would have been obvious to ordinary skill in the art at the time of the invention that the Output Queue and Transmit queue have different access times because they are called different names which implies a different media type. It would have been obvious to one of ordinary skill in the art at the time of the invention that the pointer is dequeue from the Transmit FIFO otherwise the same packet would be sent forever and the invention would not work.

In Addition Runaldue teaches:

Regarding claim 2, the reference teaches a Output Queue for the first memory and a Transmit Queue for the second memory. It would have been an obvious design choice to select a memory for the output queue which has less of an access time than for the transmit FIFO.
Regarding claim 3, the reference teaches that the transmit FIFO transfers a pointer to the data which refers to another pointer or plurality of pointer per Fig 9A and 9B which shows the next buffer pointer.
Regarding claim 5, It would have been obvious to one of ordinary skill in the art at the time of the invention that the inherent transmit logic removes the pointer when the packet has been transmitted otherwise the packets would be transmitted forever and the invention would not work.
Regarding claim 12, the Transmit FIFO has a pointer which refers to data which refers to another pointer per Figs 9A & 9B; thus, Next Buffer Pointer or Link

Referring to claim 13, Runaldue teaches: Output Queue 74 and Transmit FIFO 54 per Fig 3 or per col. 7 lines 34-52 which perform a queueing method. The Port FIFO logic writes the pointer into the Output Queue or first memory per col. 7 lines 34-52. The Buffer Manager writes the pointer into the Transmit FIFO or second per memory per col. 7 lines 34-52. Runaldue does not expressly call for: different access times associated with the Output Queue and the Transmit FIFO or dequeuing of the pointer.

It would have been obvious to ordinary skill in the art at the time of the invention that the Output Queue and Transmit queue have different access times because they are called different names which implies a different media type. It would have been obvious to one of ordinary skill in the art at the time of the invention that the pointer is dequeue from the Transmit FIFO otherwise the same packet would be sent forever and the invention would not work.

In Addition Runaldue teaches:

Regarding claim 14, the reference teaches a Output Queue for the first memory and a Transmit Queue for the second memory. It would have been an obvious design choice to select a memory for the output queue which has less of an access time than for the transmit FIFO.
Regarding claim 15, the reference teaches that the transmit FIFO transfers a pointer to the data which refers to another pointer or plurality of pointer per Fig 9A and 9B which shows the next buffer pointer.
Regarding claim 17, It would have been obvious to one of ordinary skill in the art at the time of the invention that the pointer is dequeue from the Transmit FIFO or second memory otherwise the same packet would be sent forever and the invention would not work.
Regarding claim 24, the Transmit FIFO has a pointer which refers to data which refers to another pointer per Figs 9A & 9B; thus, Next Buffer Pointer or Link to the next packet vector.

Referring to claim 25, Runaldue teaches: Output Queue 74 and Transmit FIFO 54 per Fig 3 or per col. 7 lines 34-52 which are a queue. The Output Queue 74 per Fig 3 or per col. 7 lines 34-52 is the first memory. The Transmit FIFO 54 per Fig 3 or per col. 7 lines 34-52 is the second memory. The Port FIFO logic writes the pointer into the Output Queue or first memory per col. 7 lines 34-52 (means for enqueueing). The Buffer Manager writes the pointer into the Transmit FIFO or second per memory per col. 7 lines 34-52 (means for transferring). Runaldue does not expressly call for: different access times associated with the Output Queue and the Transmit FIFO or dequeuing of the pointer.It would have been obvious to ordinary skill in the art at the time of the invention that the Output Queue and Transmit queue have different access times because they are called different names which implies a different media type. It would have been also obvious to one of ordinary skill in the art at the time of the invention that the pointer is dequeue from the Transmit FIFO (means for dequeueing) otherwise the same packet would be sent forever and the invention would not work.

In Addition Runaldue teaches:

Regarding claim 26, the reference teaches a Output Queue for the first memory and a Transmit Queue for the second memory. It would have been an obvious design choice to select a memory for the output queue which has less of an access time than for the transmit FIFO.
Regarding claim 27, the reference teaches that the transmit FIFO transfers a pointer to the data which refers to another pointer or plurality of pointer per Fig 9A and 9B which shows the next buffer pointer (means).
Regarding claim 28, the Transmit FIFO has a pointer which refers to data which refers to another pointer per Figs 9A & 9B or a plurality of pointers.
Regarding claim 30, It would have been obvious to one of ordinary skill in the art at the time of the invention that the pointer is dequeue from the Transmit FIFO or second memory otherwise the same packet would be sent forever and the invention would not work.
Regarding claim 37, the Transmit FIFO has a pointer which refers to data which refers to another pointer per Figs 9A & 9B; thus, Next Buffer Pointer or Link

Referring to claim 38, Runaldue teaches: Output Queue 74 and Transmit FIFO 54 per Fig 3 or per col. 7 lines 34-52 which are an apparatus. The Output Queue 74 per Fig 3 or per col. 7 lines 34-52 is the first memory. The Transmit FIFO 54 per Fig 3 or per col. 7 lines 34-52 is the second memory.

The Port FIFO logic writes the pointer into the Output Queue or first memory per col. 7 lines 34-52. The Buffer Manager writes the pointer into the Transmit FIFO or second per memory per col. 7 lines 34-52 (Control logic). Runaldue does not expressly call for: different access times associated with the Output Queue and the Transmit FIFO or removing the pointer form the pointer list by reading the pointer from the Output Queue or first memory.

It would have been obvious to ordinary skill in the art at the time of the invention that the Output Queue and Transmit queue have different access times because they are called different names which implies a different media type. It would have been obvious to one of ordinary skill in the art at the time of the invention pointer is removed by inherent logic (Control logic) from the Output Queue or first memory otherwise the Output Queue would have the pointer in it queue which would be output to the Transmit FIFO forever and the invention would not work.

In Addition Runaldue teaches:

Regarding claim 39, the Transmit FIFO has a pointer which refers to data which refers to another pointer per Figs 9A & 9B; thus, Next Buffer Pointer or Link in queue
Regarding claim 41, the Transmit FIFO has a pointer which refers to data which refers to another pointer per Figs 9A & 9B; thus, Next Buffer Pointer or Link to the next packet vector in the queue.
Regarding claim 42, the Transmit FIFO or second memory has a pointer which refers to data which refers to another pointer per Figs 9A & 9B; thus, Next Buffer Pointer or Link to the next packet vector in the queue.

3. Claims 43-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Runaldue (U.S. Patent No.: 6,128,654) in view of Hall (U.S. Patent No.; 6,021,325)

Referring to claim 43, Runaldue teaches: the queue of claim 1. Runaldue does not expressly call for: first memory is static RAM and the second memory is dynamic RAM but teaches first memory is a queue and second memory is a FIFO. Hall teaches that queue can be SRAM and FIFO can be DRAM per col. 2 lines 60-67. It would have been obvious to one of ordinary skill in the art at the time of the invention to add the SRAM and DRAM of Hall to the first and second memory of Runadue because they are types of memory which are well known in the art.

Referring to claim 44, Runaldue teaches: the queue method of claim 13. Runaldue does not expressly call for: first memory is static RAM and the second memory is dynamic RAM but teaches first memory is a queue and second memory is a FIFO. Hall teaches that queue can be SRAM and FIFO can be DRAM per col. 2 lines 60-67. It would have been obvious to one of ordinary skill in the art at the time of the invention to add the SRAM and DRAM of Hall to the first and second memory of Runadue because they are types of memory which are well known in the art.

Referring to claim 45, Runaldue teaches: the apparatus of claim 45. Runaldue does not expressly call for: first memory is static RAM and the second memory is dynamic RAM but teaches first memory is a queue and second memory is a FIFO. Hall teaches that queue can be SRAM and FIFO can be DRAM per col. 2 lines 60-67. It would have been obvious to one of ordinary skill in the art at the time of the invention to add the SRAM and DRAM of Hall to the first and second memory of Runadue because they are types of memory which are well known in the art.

Claim Objections

4. Claims 4, 6-11, 16, 18-23, 29, 31-36, & 40 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

5. Applicant's arguments filed 7/22/05 have been fully considered but they are not persuasive.

The examiner respectively disagrees with the applicant's argument that the reference Runaldue fails to teach "control logic which enqueues in the queue a pointer to a data to be transmitted by writing the pointer in the first memory, transfers the pointer to the second memory and dequeues the pointer from the second memory.

Runaldue teaches: The Output Queue 74 per Fig 3 or per col. 7 lines 34-52 is the first memory. The Transmit FIFO 54 per Fig 3 or per col. 7 lines 34-52 is the second memory.

The Port FIFO logic writes the pointer into the Output Queue or first memory per col. 7 lines 34-52 (control logic). The Buffer Manager writes the pointer into the Transmit FIFO or second per memory per col. 7 lines 34-52 (Control logic). Runaldue does not expressly call for: dequeuing the pointer

It would have been obvious to one of ordinary skill in the art at the time of the invention pointer is removed by inherent logic (Control logic) from the Transmit FIFO or second memory otherwise the packet would have been output forever and the invention would not have worked.

Since the examiner has changed his mind about the allowability of the previously objected claims the examiner is making this action non-final in order to give the applicant time to respond to the rejection.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert W. Wilson whose telephone number is 571/272-3075. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chau T. Nguyen can be reached on 571/272-3126. The fax phone number for the organization where this application or proceeding is assigned is 571/273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Robert W. Wilson

Robert W Wilson
Examiner
Art Unit 2661

RWW
8/11/05

BOB PHUNKULH
PRIMARY EXAMINER